EE/CprE/SE 491 WEEKLY REPORT 6

Date: ***Mar 6th, 2023 – Mar 12th, 2023***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Weekly Summary

This week we began working on a 1-bit DAC and a 1-bit ADC. The idea behind doing this was so that we were able to get practice in going through the analog process flow. This flow includes creating a schematic using XSchem, simulating the schematic with NGSpice, creating a layout, and passing an LVS check. We were able to begin this process, but inevitably we ran into issues with some of the tools. However, we were able to further understand the tools and how to use them effectively. Outside of going through the analog process flow, we began learning more about how a ReRam Crossbar works and how they are built.

Past week accomplishments

- Joshua Thater
    - Created an inverter schematic using Xschem and simulated it using NGSpice
    - Extracted Spice netlist into Magic and created a layout
    - Ran LVS check to compare two netlists
    - Continued to write documentation on tool usage
- Aiden Petersen
    -
- Matt Ottersen
    -

- Regassa Dukele
    - Working on understanding to create ADC schematic

Pending issues

- Creating a sample project to simulate and pass precheck with
- Getting LVS check to pass
- Learning more about how to use the tools effectively

Individual contributions

Team Member	Individual Contributions	Weekly Hours	Total Hours
Joshua Thater	Worked on 1-bit DAC through the analog process flow	9	40
Aiden Petersen			27
Matt Ottersen			27
Regassa Dukele	Reading about ADC to design	3	31.5

Plans for the upcoming week

- Joshua Thater
    - Getting LVS check to pass
    - Finish documentation on basics of XSchem, NGSpice, Magic, and Netgen
    - Continue through the process flow to simulate and precheck 1-bit DAC
- Aiden Petersen
    -
- Matt Ottersen
    -
- Regassa Dukele
    - Create an ADC schematic.
    - Ran LVS and netlist comparison.